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**1. SoC/CPU Core to DLA interface**

In the current SoC design, the CPU can only access the DDR through the SoC-DLA interface and DLA-DDR interface. In another word, the DDR is an exclusive slave of the DLA.

In order to achieve the abovementioned function, the RTL for SoC<->DLA on-chip memory <->DDR is added in DLA RTL design.

**2. Fix the clock-gating bug in DLA computation logic.**

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In the above diagram, if only multiplication output is selected (out1 enable), the changing data of Mul\_Out\_R would introduce dynamical power in the adder. Another register should buffer the addition operand.